CLAIMS

1. A method of manufacturing a trench gate semiconductor device comprising the steps of:

providing a silicon device body (1) having a first major surface (22), the silicon device body having a drain region (2, 4) of a first conductivity type and a body region (6) over the drain region;

forming a trench (8) extending downwards into the silicon device body (1) from the first major surface (22), the trench having sidewalls (28) and a base (29);

depositing a nitride liner (50) within the trench to protect the sidewalls;

forming a polysilicon plug (26) at the base (29) of the trench (8);

thermally oxidising the device to oxidise the polysilicon at the bottom of the trench to form an oxide plug (30) at the base of the trench; and

depositing conductive material within the trench to form a gate.

2. A method according to claim 1 wherein the step of forming a polysilicon plug (26) at the base (29) of the trench (8) forms a doped polysilicon plug at the base of the trench.

3. A method according to claim 2 wherein the step of depositing a doped polysilicon plug (26) at the base (29) of the trench (8) includes depositing polysilicon (52) over the first major surface including the trench (8) and then etching back the doped polysilicon (52) to remove the doped polysilicon from the first major surface (22) leaving the polysilicon at the base (29) of the trench.

4. A method according to claim 2 wherein the step of depositing doped polysilicon includes depositing undoped polysilicon (52) and then carrying out a diffusion process to dope the undoped polysilicon.

5. A method according to any preceding claim further comprising the steps of:

thermally oxidising the side wall of the trench to form an oxide layer (32) before depositing the nitride liner (50) over the oxide layer;

etching away the nitride liner (50) and the oxide layer (32) after oxidising the polysilicon; and

thermally oxidising the sidewalls to form a thermal oxide gate insulator (12) before depositing conductive material within the trench to form a gate.

6. A method according to any preceding claim wherein the step of forming the trench (8) includes providing a mask (20) on the first major surface defining an opening (24) and etching through the opening (24) a trench (8) extending downwards from the first major surface (22).

7. A method according to claim 6 wherein the mask (20) is an oxide hard mask.

8. A method according to any preceding claim wherein the step of depositing conductive material to form a gate includes filling the trench (8) with polysilicon to form a gate (34).

9. A method according to any preceding claim further comprising forming a source implant (14) of first conductivity type at the first major surface adjacent to the trench and forming source (36), gate (38) and drain (40) electrodes attached to the source implant (14), the gate (34) and the drain region (2, 4) respectively to complete the trench gate semiconductor device.

10. A trench MOSFET comprising:

a drain (2, 4) region of first conductivity type;

a body (6) region over the drain region;

a trench (8) extending from a first major surface through the body region;

source regions (14) laterally adjacent to the trench at the first major surface;

thermal gate oxide (12) on the side walls of the trench;

a gate electrode (34) in the trench insulated from the body region by the gate oxide;

characterised by a thick oxide plug (34) formed of oxidised doped polysilicon at the base of the trench extending into the drain region.